FEATURES

- **Low output voltage noise: 3uV$_{RMS}$**
- **Input voltage Range:**
  - **1.1V to 6.5V with Bias**
  - **1.4V to 6.5V without Bias**
- **Output voltage range:**
  - **0.5V to 5.15V using resistor divider**
  - **0.5V to 3.65V using Out Voltage Setting Pins**
- **Power supply ripple rejection: 40dB at 500kHz**
- **Low dropout voltage: 180mV at 3A**
- **±1%(max) output voltage accuracy over line, load and temperature**
- Fast transient response
- Programmable soft start
- Enable control input
- Power good indicator
- RoHS compliant and halogen free

APPLICATIONS

- High speed analog circuits: ADCs, DACs, VCOs and LVDS
- Wireless infrastructure: Serdes, FPGA, DSP
- Instrumentation, medical, and Audio
- Portable electronic devices

DESCRTION

The **XPL3233** is a low noise(3uV$_{RMS}$), high accuracy (±1%), high current(3A), low dropout (180mV) linear regulator (LDO). Output voltage of this device is programmable from 0.5V to 5.15V using external resistor divider and adjustable from 0.5V to 3.65V with OUT voltage setting pins. The device supports input voltage as low as 1.1V while there is a bias.

The low noise, high PSRR and high current capability make XPL3233 ideal to power noise sensitive circuits such as RF components, analog to digital converters (ADCs), and digital to analog converters (DACs). The low dropout voltage, remote sensing, excellent transient response, wide input and output volage range make XPL3233 suitable for powering application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGAs) and digital signal processors (DSPs).

The enable control and power good indicator function provide sequence control capability. With NR/SS pin, the noise immunity is enhanced by adding a bypass capacitor. This device is offered in a 20-Pin, QFN 3.5-mm x 3.5-mm package.

TYPICAL APPLICATION

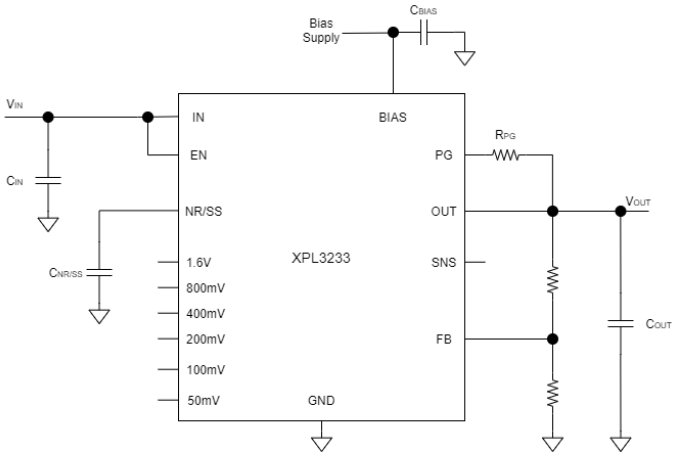


Figure 1. Typical Application Circuit

REVISON HISTORY

Table 1. Revision History

Release	Rev	Changes	Date
Preliminary	0.8	Update current limit and thermal resistance	7/10/22
Updates	0.9	Update thermal resistance (junction to case bottom)	8/25/22

ORDERING INFORMATION

Table 2. Ordering information

Part Number	Op Temp (°C)	Top Marking	Package	MOQ
XPL3233YA	-40 to +125	L3233	QFN-20 3.5-mm x 3.5-mm	5,000

MOQ = Minimum Order Quantity.
For production orders greater than MOQ, the order must be a multiple of MOQ per package size above.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

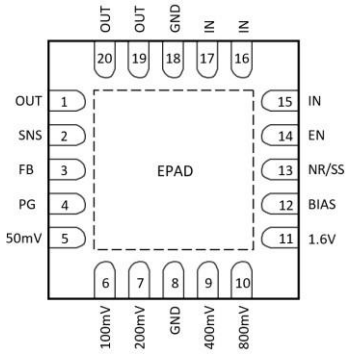


Figure 2. Pin Configuration

Table 3. Pin Definition

P IN			DESCRIPTION
NAME	**NO.**	**I/O**	
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	5, 6, 7, 9, 10, 11	I	Output voltage setting pins. These pins connect to an internal feedback network. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name. Multiple pins may be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the V_{OUT} voltage is set by external resistor.
BIAS	12	I	BIAS supply voltage. This pin enables the use of low-input voltage, low-output voltage conditions to reduce power dissipation across the die. The use of a BIAS voltage improves DC and AC performance for $V_{IN} \leq 2.2$ V. A 10-µF or larger value capacitor must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
EN	14	I	Enable pin. Driving this pin to logic high enables the device. Driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS.
FB	3	I	Feedback pin connected to the error amplifier. This pin is used to set the desired output voltage via an external resistive divider. Although not required, it is recommended to place a 10-nF feedforward capacitor from FB to OUT (as close to the device as possible) to maximize AC performance.
GND	8, 18	—	Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection.
IN	15, 16, 17	I	Input supply voltage pin. A 10µF or larger ceramic capacitor (5µF of capacitance or greater) from IN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible.
NR/SS	13	—	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces the reference voltage noise and also enables the soft-start function. Although not required, a 10-nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize AC performance.
OUT	1, 19, 20	O	Regulated output pin. A 47µF or larger ceramic capacitor (25µF of capacitance or greater) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.
PG	4	O	Active-high power-good pin. An open-drain output indicates when the output voltage reaches PG rising threshold.
SNS	2	I	Output voltage sense pin. This pin connects the internal R_0 resistor to the output. Connect this pin to the load side of the output trace only if the V_{OUT} programming pins feature is used. If using external resistor divider to set output voltage, leave this pin floating.
EPAD		—	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

ABSOLUTE MAXIMUM RATINGS

Table 4. Maximum Ratings (1)

Parameter	Min	Max	Units
IN, BIAS, EN, PG	-0.3	+7.0	V
OUT, SNS	-0.3	V_{IN} + 0.3	V
NR/SS, FB	-0.3	+3.6	V
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	-0.3	min (V_{OUT} + 0.3, 6)	V
Storage Temperature Range	-65	+150	°C
Operating Temperature	-40	+125	°C
Electrostatic Discharge (HBM)	-2000	+2000	V
Electrostatic Discharge (CDM)	-1000	+1000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Table 5. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Input Supply Voltage	V_{IN}	1.1(1)		6.5	V
Bias Supply Voltage Range	V_{BAIS}	3		6.5	V
Output Voltage Range	V_{OUT}(2)	0.5		5.15	V
Output Current	I_{OUT}	0		3	A
Input capacitor	C_{IN}	10	47		µF
Output capacitor	C_{OUT}	47	47 || 10 || 10(3)		µF
Power-good pullup resistance	R_{PG}	10		100	kΩ
NR/SS capacitor	$C_{NR/SS}$		10		nF
Feed-forward capacitor	C_{FF}		10		nF
Top resistor value in feedback network for adjustable operation	R_1		12.1(4)		kΩ
Bottom resistor value in feedback network for adjustable operation	R_2			160(5)	kΩ
Operating junction temperature	T_J	–40		125	°C

(1) BIAS supply is required when the VIN supply is below 1.4 V. Conversely, no BIAS supply is required when the VIN supply is higher than or equal to 1.4 V. A BIAS supply helps improve DC and AC performance for VIN ⩽ 2.2 V.
(2) This output voltage range does not include device accuracy or accuracy of the feedback resistors.
(3) The recommended output capacitors are selected to optimize PSRR for the frequency range of 400 kHz to 700 kHz. This frequency range is a typical value for dc-dc supplies.
(4) The 12.1-kΩ resistor is selected to optimize PSRR and noise by matching the internal R1 value.
(5) The upper limit for the R2 resistor is to ensure accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.

Table 6. Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Thermal Resistance Junction-to-Ambient	θ_{JA}	27.0	°C/W
Thermal Resistance Junction-to-Case (top)	$\theta_{JC(top)}$	15.5	°C/W
Thermal Resistance Junction-to-Case (bottom)	$\theta_{JC(bot)}$	3.5	°C/W

ELECTRICAL SPECIFICATIONS

Over operating junction temperature range (TJ = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.5 V[1], I_{OUT} = 10mA, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, without $C_{NR/SS}$ and C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C.

Table 7.

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Input supply UVLO with BIAS	$V_{UVLO1(IN)}$	V_{IN} rising with V_{BIAS} = 3.0 V			1.02	1.085	V
$V_{UVLO1(IN)}$ hysteresis	$V_{HYS1(IN)}$	V_{BIAS} = 3.0 V			100		mV
Input supply UVLO without BIAS	$V_{UVLO2(IN)}$	V_{IN} rising			1.31	1.39	V
$V_{UVLO2(IN)}$ hysteresis	$V_{HYS2(IN)}$				100		mV
Bias supply UVLO	$V_{UVLO(BIAS)}$	V_{BIAS} rising, V_{IN} = 1.1 V			2.4	2.9	V
$V_{UVLO(BIAS)}$ hysteresis	$V_{HYS(BIAS)}$	V_{IN} = 1.1 V			300		mV
Bias supply voltage range	V_{BIAS}	V_{IN} = 1.1 V		3.0		6.5	V
BIAS pin current	I_{BIAS}	VIN = 1.1 V, VBIAS = 6.5 V, VOUT(nom) = 0.5 V, I_{OUT} = 3 A			15		mA
GND pin current	I_{GND}	V_{IN} = 6.5 V, I_{OUT} = 5 mA			15		mA
		V_{IN} = 1.4 V, I_{OUT} = 3 A			15		mA
		Shutdown, PG = open, V_{IN} = 6.5 V, V_{EN} = 0.5 V			7		µA
Feedback voltage	V_{FB}				0.5		V
FB pin leakage current	I_{FB}	V_{IN} = 6.5 V		–100		100	nA
NR/SS pin voltage	$V_{NR/SS}$				0.5		V
NR/SS pin charging current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 6.5 V		4.0	6.6	9.0	µA
Output voltage[3]	V_{OUT}	Using the pin programming		0.5 – 1%		3.65 + 1%	V
		Using external resistors[2]		0.5 – 1%		5.15 + 1%	V
		0.5 V ≤ V_{OUT} ≤ 5.15[4] V, 5 mA ≤ I_{OUT} ≤ 3 A, over V_{IN}		–1%		1%	
		V_{IN} = 1.1 V, V_{OUT} = 0.5V, 5 mA ≤ I_{OUT} ≤ 3 A, 3.0 V ≤ V_{BIAS} ≤ 6.5 V		–1%		1%	
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 5 mA, 1.4 V ≤ V_{IN} ≤ 6.5 V			0.05		%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	5 mA ≤ I_{OUT} ≤ 3 A			0.08		%/A
Dropout Voltage	V_{DO}	V_{IN} = 1.1V to 6.5V, I_{OUT} = 3 A, V_{FB} = 0.5 V – 3%			120	180	mV
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.75 V, V_{BIAS} = 3.6 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF			3		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{OUT} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF			8.3		
PSRR	Power-supply ripple rejection	V_{IN} – V_{OUT} = 0.4 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 22 µF	f = 10 kHz, V_{OUT} = 0.75 V, V_{BIAS} = 5.0 V		65		dB
			f = 500 kHz, V_{OUT} = 0.75 V, V_{BIAS} = 5.0 V		40		
			f = 10 kHz, V_{OUT} = 5.0 V		59		
			f = 500 kHz,		25		

		V_{OUT} = 5.0 V				
Output Current Limit	I_{LIM}		3.5	4.2	6.5	A
EN pin high-level input voltage	$V_{IH(EN)}$		1.1		6.5	V
EN pin low-level input voltage	$V_{IL(EN)}$		0		0.5	V
EN pin current	I_{EN}	V_{IN} = 6.5 V, V_{EN} = 0 V and 6.5 V	-0.1		0.1	µA
PG pin threshold	$V_{PG\_FALLING}$	For falling V_{OUT}	82% x V_{OUT}	88% x V_{OUT}	93% x V_{OUT}	V
PG pin hysteresis	V_{PG_HYS}	For rising V_{OUT}		2% x V_{OUT}		V
PG pin low-level output voltage	V_{PG_OL}	V_{OUT} < $V_{PG\_FALLING}$, I_{PG} = –1 mA			0.4	V
PG pin leakage current	I_{PG_LK}	V_{OUT} > $V_{PG\_FALLING}$ + V_{PG_HYS}, V_{PG} = 6.5 V			1	µA
Thermal shutdown temperature	T_{SD}	Shutdown, temperature increasing		150		°C
		Reset, temperature decreasing		130		
Operating junction temperature	T_J		-40		125	°C

(1) $V_{OUT(nom)}$ is the calculated V_{OUT} target value from the pin programmable in a fixed configuration. In an adjustable configuration, $V_{OUT(nom)}$ is the expected V_{OUT} value set by the external feedback resistors.

(2) When the device is connected to external feedback, resistors at the FB pin, external resistor tolerances are not included.

(3) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.7 V and I_{OUT} = 3 A, because the power dissipation is higher than the maximum rating of the package.

(4) For V_{OUT} ≤ 5V, V_{IN} = V_{OUT} + 0.4V; For V_{OUT} > 5V, V_{IN} = V_{OUT} + 0.45V

TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

THEORY OF OPERATION

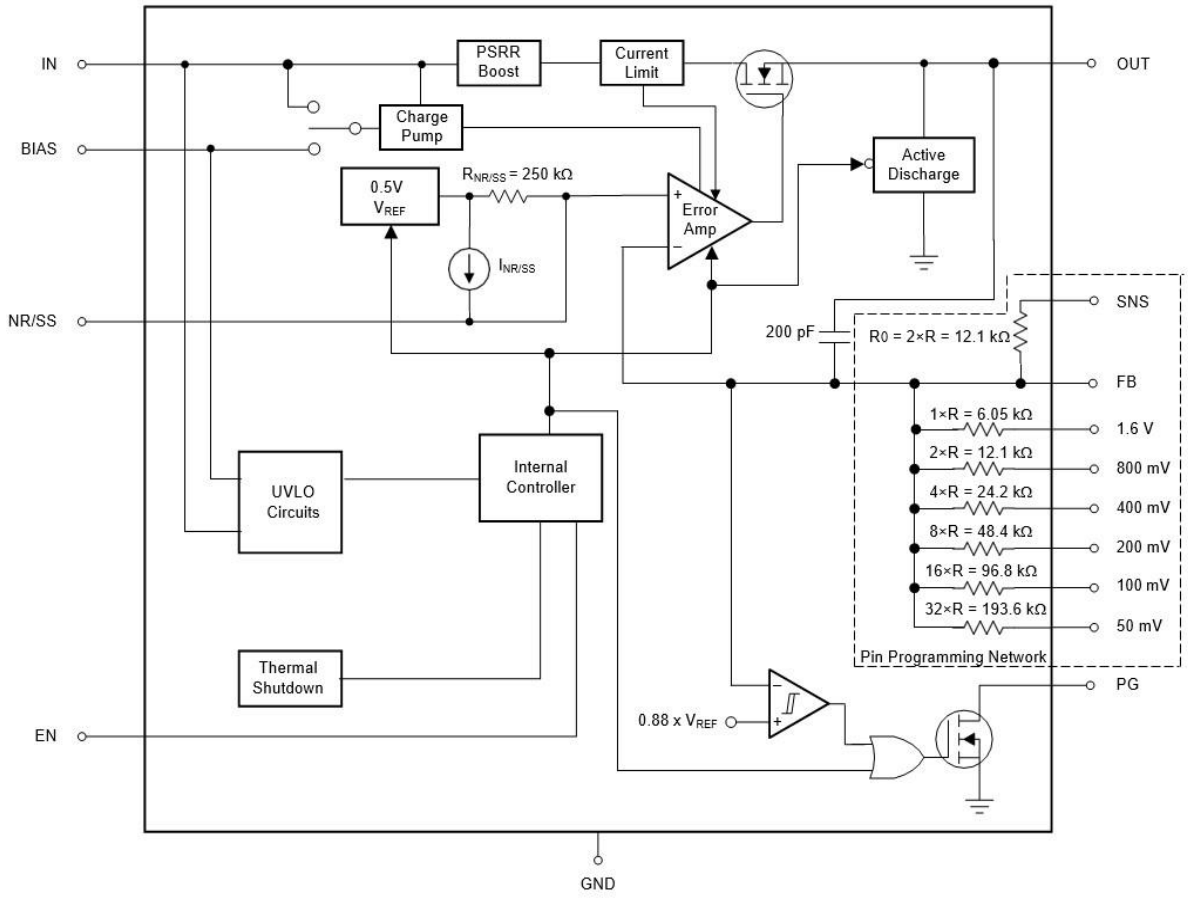


Figure 3. XPL3233 Block Diagram

The **XPL3233** is a low noise($3uV_{RMS}$), high accuracy (1%), high current(3A), low dropout (180mV) linear voltage regulator (LDO). With the excellent performance and practical features, XPL3233 provides a clean and accurate power supply for many applications.

A low-noise reference and error amplifier are included to reduce device noise. The NR/SS capacitor filters the noise from the reference and feed-forward capacitor filters the noise from the error amplifier. The high Power-Supply-Rejection-Ratio (PSRR) of the XPL3233 minimizes the coupling of input supply noise to the output.

ENABLE AND SHUTDOWN

The XPL3233 provides an EN pin, as an external chip enable control, to enable or disable the device. The regulator is turned off and enters the shutdown mode when V_{EN} is below 0.5V. When V_{EN} is above 1.1V, the regulator is turned on. When the regulator is shut down, the ground current is reduced to typical 7μA.

If the enable timing control is not used, connect EN to the largest capacitance on the input as close as possible to prevent voltage droops on the VIN line from triggering the enable circuit.

VOUT PROGRAMMING PINS

The XPL3233 has built-in matched feedback resistor network to set output voltage. The output voltage can be programmed from 0.5V to 3.65V in 50mV steps when tying these programming pins (Pins 5 to 11) to ground. Tying any of the V_{OUT} programming pins to SNS can lower the value of the upper resistor divider. Hence, the V_{OUT} programming resolution is increased. See details in Output Voltage Setting.

PROGRAMMABLE SOFT START

The noise-reduction capacitor ($C_{NR/SS}$) accomplishes dual purpose of noise-reduction and programming the soft-start ramp time during turn-on. When V_{EN} and V_{UVLO} exceeds the respective threshold voltage, the XPL3233 activates a quick start circuit to charge the noise reduction capacitor ($C_{NR/SS}$) and then the output voltage ramps up.

POWER GOOD

The power good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open drain PG pin requires an external pull-up resistor to an external supply, any downstream device can receive power good as a logic signal that can be used for sequencing. The pull-up resistor from 10kΩ to 100kΩ is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving devices.

After start-up, the PG pin becomes high impedance when the feedback voltage exceeds V_{PG_HYS} (typically 90% of 0.5V reference voltage level). The PG is pulled to GND when the feedback pin voltage falls below the $V_{PG\_FALLING}$, V_{EN} low, current limit and over temperature protection.

UNDER VOLTAGE LOCKOUT (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{IN} rises above the V_{UVLO} threshold and V_{BIAS} rises above the V_{BIAS_UVLO}. The UVLO circuit also disables the output of the device when V_{IN} and V_{BIAS} falls below the lockout voltage hysteresis. The UVLO circuit is activated to disable the output of the device if V_{IN} or V_{BIAS} drops.

INTERNAL CURRENT LIMIT (ILIM)

The XPL3233 continuously monitors the output current to protect the power switch against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the power switch gate voltage to turn off the pass transistor.

Thermal shutdown can be activated during a current limit event because of the high power-dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances of the input and load. Continuous operating in current limit is not recommend.

By reason of the build-in body diode, the power switch conducts current when the output voltage exceeds input voltage. Since the current is not limited, external current protection should be added if the device may work at reverse voltage state. See details in Reverse Current Protection.

OVER TEMPERATURE PROTECTION (OTP)

The XPL3233 implements thermal shutdown protection. The device is disabled when the junction temperature (T_J) exceeds 150°C (typical). The LDO automatically turns on again when the temperature falls by 20°C (typical).

For reliable operation, limit the junction temperature to a maximum of 125°C. Continuously running the XPL3233 into thermal shutdown or above junction temperature of 125°C reduces long-term reliability.

OUTPUT ACTIVE DISCHARGE

When the device is disabled, the XPL3233 discharges the LDO output (via OUT pins) through an internal several hundred ohms impedance to ground. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. External current protection should be added if the device may work at reverse voltage state.

APPLICATION INFORMATION

The XPL3233 is a high current, low-noise, high accuracy, low-dropout linear regulator which is capable of sourcing 3A with only maximum 180mV dropout. The input voltage operating range is from 1.1V to 6.5V, and the adjustable output voltage is from 0.5V to 5.15V by setting external resistor or from 0.5V to 3.65V by shorting specific pins on PCB layout to get required output target.

OUTPUT VOLTAGE SETTING

The output voltage of the XPL3233 can be set by external resistors or by output voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV and 1.6V) to achieve different output targets.

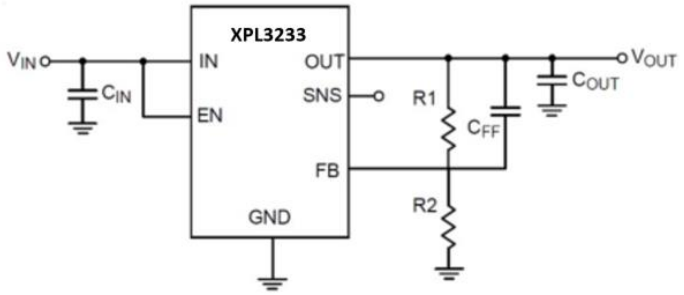
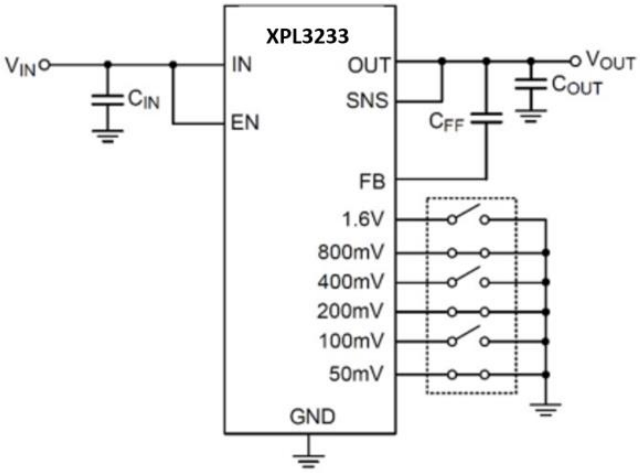


Figure 4. Output Voltage Set by External Resistor

By using external resistors, the output voltage is determined by the values of R1 and R2 as **Figure 4**. The values of R1 and R2 can be calculated by the formula below.

$$V_{OUT} = 0.5V \times \frac{R_1 + R_2}{R2}$$



V_{OUT} = 0.5V + (∑ Output setting pins to Ground)

= 0.5V + (0.8V + 0.2V + 0.05V) = 1.55V

Figure 5. Output Voltage Setting without External Resistors

The XPL3233 also can short the pins 5, 6, 7, 9, 10 and 11 to ground to program the regulated output voltage level without external resistors after the SNS pin is connected to the OUT pin. The pins 5, 6, 7, 9, 10 and 11 are connected to internal resistor pairs, and each pin is either connected to ground (active) or left open (floating).

The voltage programming is set as the sum of the internal reference voltage (V_{REF} = 0.5V) plus the accumulated sum of the inspective voltages assigned to each active pin as illustrated in **Figure 5**.

Table 8 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open or floating, the output is thereby programmed to the minimum possible output voltage which equals to V_{REF} (0.5V). The maximum output target can be supported up to 3.65V after all pins 5, 6, 7, 9, 10 are shorted to ground at the same time.

Table 8. Output Voltage with Pin Programming

V_{OUT}(V)	50mV	100mV	200mV	400mV	800mV	1.6V	V_{OUT}(V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.5	Open	Open	Open	Open	Open	Open	2.1	Open	Open	Open	Open	Open	GND
0.55	GND	Open	Open	Open	Open	Open	2.15	GND	Open	Open	Open	Open	GND
0.6	Open	GND	Open	Open	Open	Open	2.2	Open	GND	Open	Open	Open	GND
0.65	GND	GND	Open	Open	Open	Open	2.25	GND	GND	Open	Open	Open	GND
0.7	Open	Open	GND	Open	Open	Open	2.3	Open	Open	GND	Open	Open	GND
0.75	GND	Open	GND	Open	Open	Open	2.35	GND	Open	GND	Open	Open	GND
0.8	Open	GND	GND	Open	Open	Open	2.4	Open	GND	GND	Open	Open	GND
0.85	GND	GND	GND	Open	Open	Open	2.45	GND	GND	GND	Open	Open	GND
0.9	Open	Open	Open	GND	Open	Open	2.5	Open	Open	Open	GND	Open	GND
0.95	GND	Open	Open	GND	Open	Open	2.55	GND	Open	Open	GND	Open	GND
1	Open	GND	Open	GND	Open	Open	2.6	Open	GND	Open	GND	Open	GND
1.05	GND	GND	Open	GND	Open	Open	2.65	GND	GND	Open	GND	Open	GND
1.1	Open	Open	GND	GND	Open	Open	2.7	Open	Open	GND	GND	Open	GND
1.15	GND	Open	GND	GND	Open	Open	2.75	GND	Open	GND	GND	Open	GND
1.2	Open	GND	GND	GND	Open	Open	2.8	Open	GND	GND	GND	Open	GND
1.25	GND	GND	GND	GND	Open	Open	2.85	GND	GND	GND	GND	Open	GND
1.3	Open	Open	Open	Open	GND	Open	2.9	Open	Open	Open	Open	GND	GND
1.35	GND	Open	Open	Open	GND	Open	2.95	GND	Open	Open	Open	GND	GND
1.4	Open	GND	Open	Open	GND	Open	3	Open	GND	Open	Open	GND	GND
1.45	GND	GND	Open	Open	GND	Open	3.05	GND	GND	Open	Open	GND	GND
1.5	Open	Open	GND	Open	GND	Open	3.1	Open	Open	GND	Open	GND	GND
1.55	GND	Open	GND	Open	GND	Open	3.15	GND	Open	GND	Open	GND	GND
1.6	Open	GND	GND	Open	GND	Open	3.2	Open	GND	GND	Open	GND	GND
1.65	GND	GND	GND	Open	GND	Open	3.25	GND	GND	GND	Open	GND	GND

V_{OUT}(V)	50mV	100mV	200mV	400mV	800mV	1.6V	V_{OUT}(V)	50mV	100mV	200mV	400mV	800mV	1.6V
1.7	Open	Open	Open	GND	GND	Open	3.3	Open	Open	Open	GND	GND	GND
1.75	GND	Open	Open	GND	GND	Open	3.35	GND	Open	Open	GND	GND	GND
1.8	Open	GND	Open	GND	GND	Open	3.4	Open	GND	Open	GND	GND	GND
1.85	GND	GND	Open	GND	GND	Open	3.45	GND	GND	Open	GND	GND	GND
1.9	Open	Open	GND	GND	GND	Open	3.5	Open	Open	GND	GND	GND	GND
1.95	GND	Open	GND	GND	GND	Open	3.55	GND	Open	GND	GND	GND	GND
2	Open	GND	GND	GND	GND	Open	3.6	Open	GND	GND	GND	GND	GND
2.05	GND	GND	GND	GND	GND	Open	3.65	GND	GND	GND	GND	GND	GND

POWER SUPPLY RECOMMENDATIONS

The XPL3233 device is designed to operate from an input voltage supply range from 1.1 V to 6.5 V. If the input supply is less than 1.4 V, then a bias rail of at least 3 V must be applied at BIAS pin. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR may help improve output noise performance.

DROPOUT VOLTAGE

The dropout voltage refers to the voltage difference between the IN and OUT pins while operating at specific output current. The dropout voltage V_{DO} also can be expressed as the voltage drop on the power switch at specific output current while the power switch is fully operating at ohmic region, and the power switch can be characterized as a resistance $R_{DS(ON)}$. Thus, the dropout voltage can be defined as ($V_{DO} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$). For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DO}$) for good transient response and PSRR performance. In other words, the performance will be degraded severely while operating at the dropout region.

INPUT AND OUTPUT CAPACITOR SELECTION

The XPL3233 is designed to support the low equivalent series resistance (ESR) ceramic capacitors. The X7R, X5R, and COG-rated ceramic capacitors are recommended due to its good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

However, the ceramic capacitance varies with operating voltage and temperature, and the design engineers must be aware of these characteristics. It is recommended to use a capacitor no less than 47µF (22µF or greater of effective capacitance) to ensure stability. The PCB trace impedance also contributes to stability for higher capacitance. If a higher capacitance (> 22µF) is required, place the additional capacitors after 2 inches and connect with a trace width of less than 0.25 inches. The input capacitance is selected to minimize transient input droop during load current steps. For general applications, an input capacitor of at least 10µF is highly recommended for minimal input impedance. If the trace inductance between the XPL3233 and input supply is high, a fast load transient may cause input voltage level ringing and exceeds the absolute maximum voltage rating that also damage the device. Adding more input capacitors can restrict the ringing and keep it not exceeding the device absolute maximum ratings.

Place these capacitors as close to the pins as possible for optimizing performance and ensuring stability.

FEED-FORWARD CAPACITOR (C_{FF})

The XPL3233 is designed to be stable without the external feed-forward capacitor (C_{FF}). However, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can also be used, but the start-up time is longer, and the power-good signal will incorrectly indicate that the output voltage is settled.

SOFT START AND NOISE REDUCTION ($C_{NR/SS}$)

The XPL3233 is designed for a programmable, monotonic soft-start time of output rising, and it can be achieved via an external capacitor ($C_{NR/SS}$) on NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general application. It not only minimizes the in-rush current but also helps reduce the noise component from internal reference. During the monotonic start-up procedure, the error amplifier of the XPL3233 tracks the voltage ramp of the external soft-start capacitor ($C_{NR/SS}$) until the voltage approaches the internal reference 0.5V. The soft-start ramp time can be calculated by the following equation and is related to the soft start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference 0.5V (V_{REF}).

$$t_{SS} = \frac{V_{REF} \times C_{NR/SS}}{I_{NR/SS}}$$

For noise-reduction consideration, the $C_{NR/SS}$ combines conjunction with an internal noise-reduction resistor to form a low-pass filter and filters the noise from the internal bandgap reference before it is gained up via the error amplifier, thus reducing the total device noise floor.

INPUT INRUSH CURRENT

During start-up process, the input Inrush current that goes into IN pin consists of the sum of load current and the charging current of the output capacitor. The inrush current is difficult to measure because the input capacitor must be removed which is not recommended. Generally, the soft-start inrush current can be estimated by the following equation, which $V_{OUT}(t)$ is the instantaneous output voltage of the power-up ramp, $dV_{OUT}(t)$ / dt is the slope of the V_{OUT} ramp, and R_{OUT} is the resistive load impedance.

$$I_{INRUSH}(t) = \frac{C_{OUT} \times dV_{OUT}(t)}{dt} + \frac{V_{OUT}(t)}{R_{OUT}}$$

UNDER VOLTAGE LOCKOUT (UVLO)

The under-voltage lockout (UVLO) threshold is the minimum input operational voltage range that ensures the device stays disabled. **Figure 6** explains the UVLO circuit is triggered between three different input voltage events (duration a, b and c), assuming $V_{EN} \geq V_{EN\_IH}$ for all time duration. For duration “a”, input power starts rising and V_{IN} exceeds the UVLO rising threshold. The V_{OUT} starts to power on then reached the target level and under regulated. Duration “b” shows a case that V_{IN} occurs instant power line unstable and droops severely. However, the V_{IN} droop level is lower than UVLO hysteresis, the device remains normal work status and V_{OUT} is still under regulated. The duration “c” happens when the V_{IN} droop level is higher than UVLO hysteresis. The control loop of device is disabled and does not have the regulation ability, and the V_{OUT} droops at the same time. For general application, instant power line transient with long power trace between IN pin and power supply may have V_{IN} level unstable which forces the device trap into duration c and makes output voltage collapse. In this case, adding more input

capacitance or improving input trace layout on PCB are effective to make sure the stability of input power stabilization.

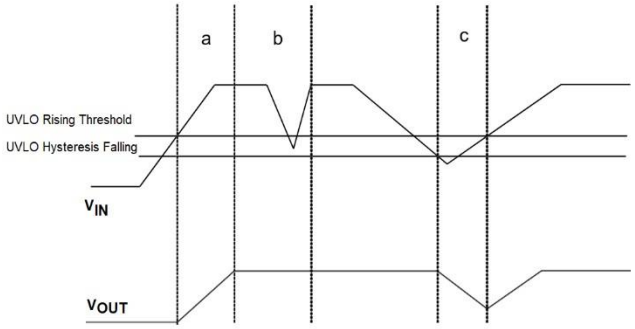


Figure 6. Under-Voltage Lockout Trigging Conditions and Output Variation

POWER GOOD (PG) FUNCTION

The power good function monitors the voltage level at the feedback pin to indicate whether the output voltage status is normal or not. The power good signal of XPL3233 as a logic signal can be used for the sequence design of the system application. The PG pin is an open-drain structure, and an external pull-up resistor is required to connect to an external supply. The pulled-up resistor value between 10kΩ to 100kΩ is recommended for proper operation. The lower limit of 10kΩ maximizes the pulled-down strength of the power good switch and the upper limit of 100kΩ minimizes the leakage current at the PG pin.

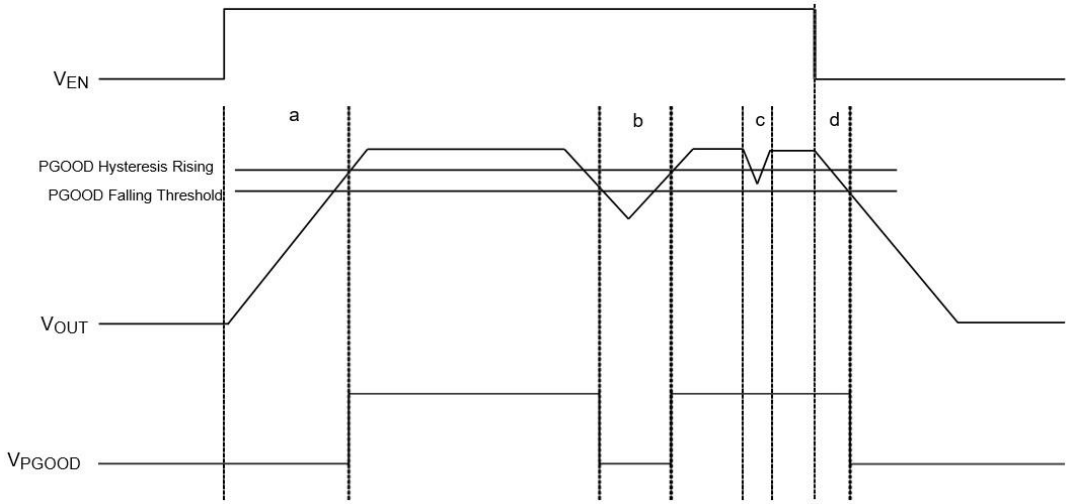


Figure 7. PG Trigger Scenario with Different Operating Status

Figure 7 demonstrates some PG scenarios versus the IN, EN and protection status. Duration “a” presents that the device is under the operation while V_{EN} is higher than V_{EN_IH} threshold. After the output voltage V_{OUT} starts rising (the rising time is related to soft-start capacitor $C_{NR/SS}$), the V_{OUT} exceeds PG hysteresis threshold, the corresponding feedback voltage V_{FB} exceeds V_{PG_HYS} threshold, and the PG pin is high impedance. The duration “b” indicates some unpredictable operation happens, for example OTP, OCP or output voltage droop severely caused by fast load step. Where the V_{FB} is lower than $V_{PG\_FALLING}$ threshold and the V_{PG} is pulled to GND for the indication that output voltage status is not ready. Duration “c” assumes V_{OUT} has small droop that is not lower than PG falling

threshold, the PG pin remains high impedance. After V_{EN} goes logic low level, V_{PG} is pulled to GND as presented in duration "d".

REVERSE CURRENT PROTECTION

If the maximum V_{OUT} exceeds V_{IN} + 0.3V, that may induce reverse current from OUT to IN which flows through the body diode of power switch instead of the normal conducting channel. In this case, the power switch may be damaged. For example, the output is biased above input supply voltage level or input supply has instant collapse at light load operation that makes $V_{IN} < V_{OUT}$. As shown in **Figure 8**, an external Schottky diode can be added to prevent the power switch from being damaged by the reverse current.

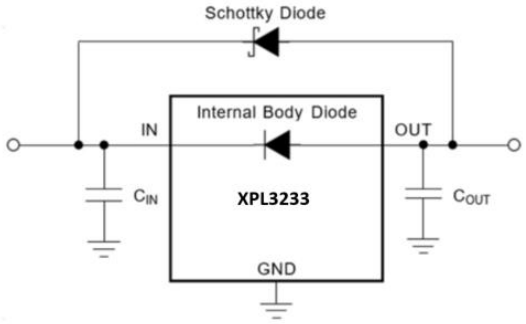


Figure 8. Application Circuit for Reverse Current Protection

THERMAL CONSIDERATIONS

Thermal protection limits power dissipation in the XPL3233. When power dissipation on power switch (P_D = (V_{IN} - V_{OUT}) x I_{OUT}) is too much that causes the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function and turns the power switch off. The power switch turns on again after the junction temperature cools down by 20°C. The XPL3233 output voltage will be closed to zero when output short circuit occurs. It reduces the chip temperature and provides maximum safety to end users when output short circuit occurs.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA})$$

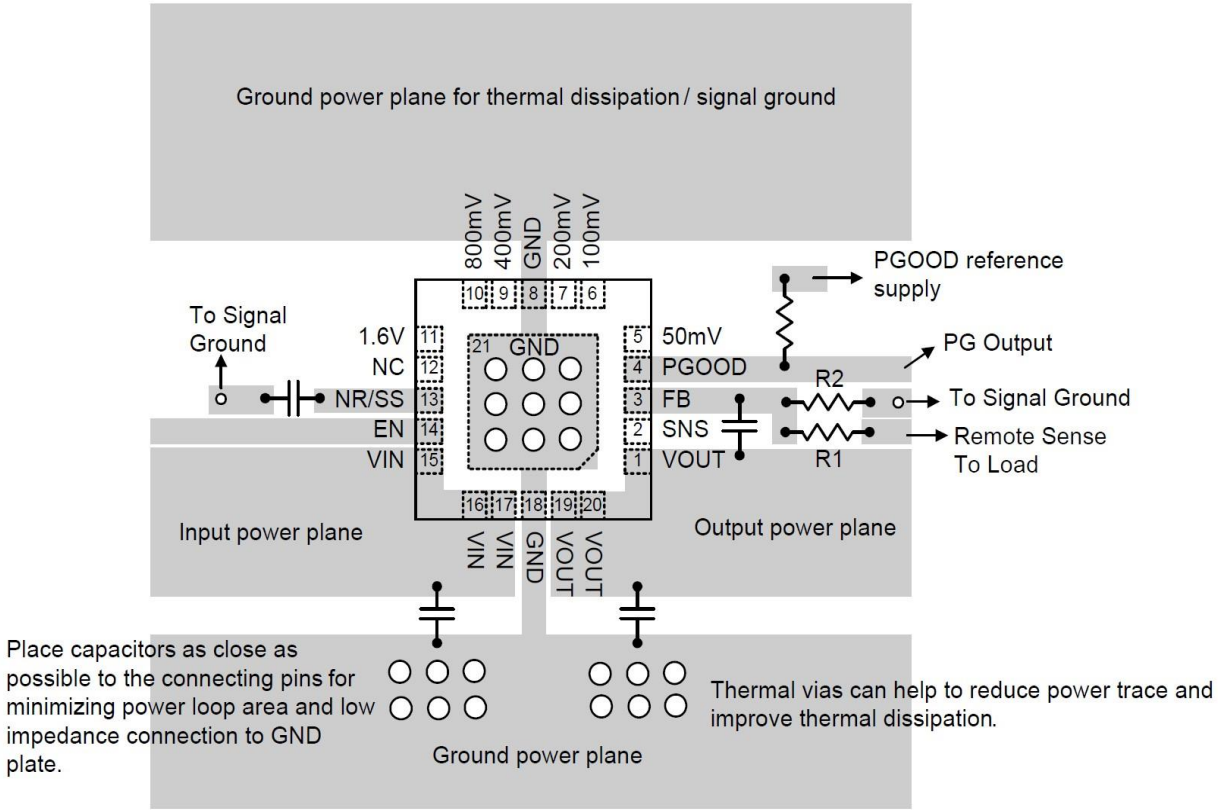
where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The maximum power dissipation will be derated with the ambient temperature rise.

For continuous operation, the maximum operating junction temperature indicated under Absolute Maximum Ratings is 125°C.

LAYOUT CONSIDERATIONS

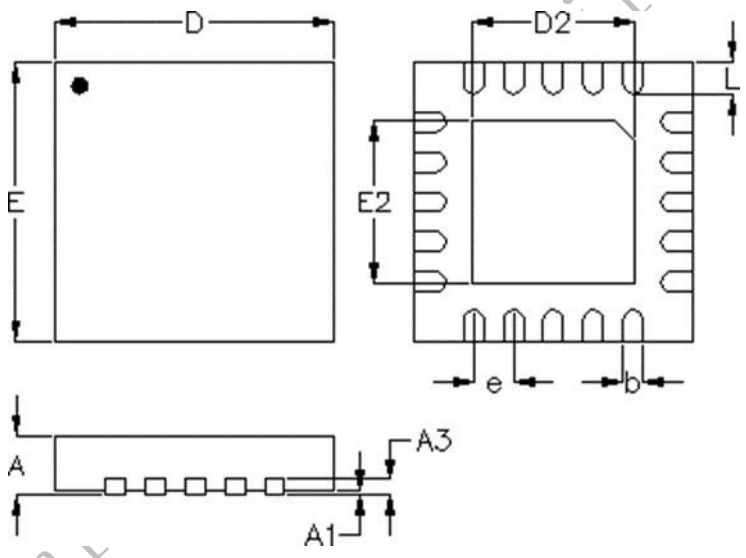
For best performance of the XPL3233, the PCB layout suggestions below are highly recommended. All circuit components should be placed on the same side and as near to the respective LDO pin as possible. The ground return path connection should be placed to the input and output capacitor, and the ground plane should be connected by a wide copper surface for good thermal dissipation. Using vias and long power traces for the input and output capacitors connection is discouraged and has negatively effects on performance. Figure 10 shows an example for the layout reference that reduces conduction trace loop, helping to minimize inductive parasitic, and keep good circuit stability.



PHYSICAL DIMENSIONS

Table 7. Chip Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203		0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.000	2.100	0.079	0.083
E	3.400	3.600	0.134	0.142
E2	2.000	2.100	0.079	0.083
e	0.500		0.020	
L	0.350	0.450	0.014	0.018



TOP MARKING