

### FEATURES

- 3-mm × 2.8-mm × 1.4-mm LGA package
- 4.5-V to 17-V input range
- 3-A continuous output current
- Advanced CoT control topology
- Power saving mode for light-load efficiency
- 40- $\mu$ A operating quiescent current
- 0.9-V to 6-V adjustable output voltage
- Power-good output
- Programmable soft start-up
- Thermal shutdown protection
- -40C to 125C operating temperature range
- EU RoHS compliance, Pb free

### APPLICATIONS

- Industrial applications
- Telecom and networking applications
- Solid state drives

### DESCRIPTION

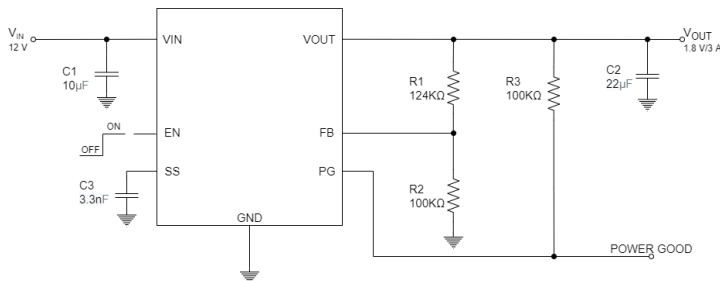
The XPM82130 is a 17-V input 3-A step-down power module optimized for small solution size and high efficiency. The module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components, and save PCB area.

The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

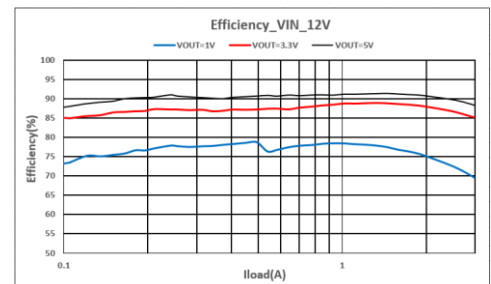
To maximize efficiency, the converter operates in PWM mode with a nominal 2MHz switching frequency and automatically enters power saving mode operation at light load currents. In power saving mode, the device operates with 40- $\mu$ A (typical) quiescent current. Using the Advanced CoT control topology, the XPM82130 achieves excellent load transient performance and accurate output voltage regulation.

### TYPICAL APPLICATION

Simplified Schematic 1.8-V Output Application



12-V Input Voltage Efficiency



## REVISION HISTORY

| Release     | Rev | Changes | Date       |
|-------------|-----|---------|------------|
| Preliminary | 0.7 | Updates | 11/01/2023 |

## ORDERING INFORMATION

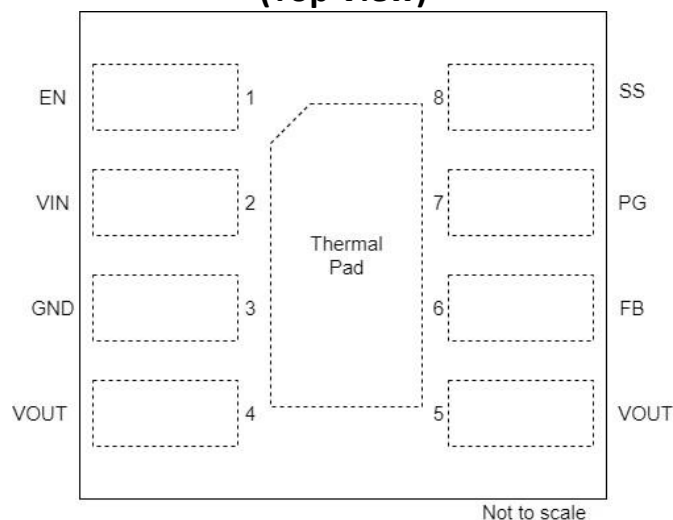
| Part Number | Output Current (A) | VOUT (V)   | Top Marking | MPQ   |
|-------------|--------------------|------------|-------------|-------|
| XPM82130    | 3                  | Adjustable | 82130       | 3,000 |
|             |                    |            |             |       |

MPQ = Minimum Packaging Quantity.

For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

## PIN CONFIGURATION AND DESCRIPTION

**8-Pin LGA Package  
(Top View)**



### Pin Configuration

| Pin  | Name                | Description                                                                                                                                                                      |
|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | EN                  | Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pull-down resistor of typically 400 k $\Omega$ when the device is disabled. |
| 2    | VIN                 | Input pin.                                                                                                                                                                       |
| 3    | GND                 | Ground pin.                                                                                                                                                                      |
| 4, 5 | VOUT                | Output pin.                                                                                                                                                                      |
| 6    | FB                  | Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.                                                                          |
| 7    | PG                  | Power good open drain output pin. A pull up resistor can be connected to any voltage less than 6 V. Leave it open if it is not used.                                             |
| 8    | SS                  | Soft startup pin. An external capacitor connected to this pin sets the internal reference voltage rising time.                                                                   |
|      | Exposed Thermal Pad | The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.                                  |

## ABSOLUTE MAXIMUM RATINGS

| Parameter                     | Min   | Max   | Units |
|-------------------------------|-------|-------|-------|
| VIN                           | -0.3  | 20    | V     |
| EN, SS                        | -0.3  | 7     | V     |
| PG, FB                        | -0.3  | 7     | V     |
| VOUT                          | -0.3  | 7     | V     |
| Sink current at PG pin        |       | 10    | mA    |
| Module operating temperature  | -40   | +125  | °C    |
| Storage temperature           | -55   | +125  | °C    |
| Electrostatic Discharge (HBM) | -2000 | +2000 | V     |
| Electrostatic Discharge (CDM) | -1000 | +1000 | V     |

<sup>(1)</sup> Operation of the device outside of these parameters may cause permanent damage.

## RECOMMENDED OPERATING CONDITIONS

| Parameter                           | Symbol           | Min | Typ | Max  | Units |
|-------------------------------------|------------------|-----|-----|------|-------|
| Input voltage                       | V <sub>IN</sub>  | 4.5 |     | 17   | V     |
| Logic Interface (EN high)           | V <sub>IH</sub>  | 0.9 |     | 6    | V     |
| Logic Interface (EN Low)            | V <sub>IL</sub>  | 0   |     | 0.33 | V     |
| Power good pull-up resistor voltage | V <sub>PG</sub>  |     |     | 6    | V     |
| Output voltage                      | V <sub>OUT</sub> | 0.9 |     | 6    | V     |
| Output current                      | I <sub>OUT</sub> | 0   |     | 3    | A     |
| Module operating temperature range  | T <sub>OJ</sub>  | -40 |     | 110  | °C    |

### Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70μm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

| Parameter                              | Symbol          | Typ  | Units |
|----------------------------------------|-----------------|------|-------|
| Junction-to-Ambient Thermal Resistance | θ <sub>JA</sub> | 50.2 | °C/W  |
| Junction-to-Case Thermal Resistance    | θ <sub>JC</sub> | 8.6  | °C/W  |

## ELECTRICAL SPECIFICATIONS

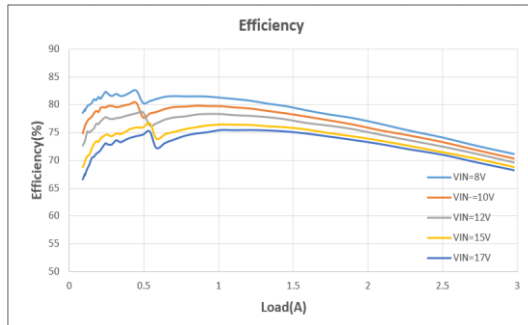
$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $V_{IN} = 4.5\text{V}$  to  $17\text{V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$  and  $V_{IN} = 12\text{V}$ , unless otherwise noted.

| Parameter                         | Symbol              | Test Condition                                 | Min  | Typ  | Max | Units |
|-----------------------------------|---------------------|------------------------------------------------|------|------|-----|-------|
| Supply                            |                     |                                                |      |      |     |       |
| Quiescent current into VIN        | I <sub>Q</sub>      | No Load, device not switching                  |      | 40   |     | uA    |
| Shutdown current into VIN         | I <sub>SD</sub>     | EN = Low                                       |      | 1.5  | 7   | uA    |
| Undervoltage lockout threshold    | V <sub>UVLO</sub>   | V <sub>IN</sub> falling                        |      | 3.8  |     | V     |
|                                   |                     | V <sub>IN</sub> rising                         |      | 4.2  | 4.5 | V     |
| Thermal shutdown threshold        | T <sub>JSD</sub>    | T <sub>J</sub> rising                          |      | 160  |     | °C    |
|                                   |                     | T <sub>J</sub> falling                         |      | 140  |     | °C    |
| Logic Interface: EN               |                     |                                                |      |      |     |       |
| High-level input voltage          | V <sub>IH</sub>     |                                                |      | 0.73 | 0.9 | V     |
| Low-level input voltage           | V <sub>IL</sub>     |                                                | 0.33 | 0.63 |     | V     |
| Input leakage current into EN pin | I <sub>lk(EN)</sub> | EN = High                                      |      | 0.01 | 1   | μA    |
| Control (SS, PG)                  |                     |                                                |      |      |     |       |
| SS pin source current             | I <sub>SS</sub>     |                                                |      | 2.5  |     | uA    |
| Power good threshold              | V <sub>PG</sub>     | V <sub>OUT</sub> rising                        | 92   | 95   | 99  | %     |
|                                   |                     | V <sub>OUT</sub> falling                       | 87   | 90   | 94  | %     |
| Power good low-level voltage      | V <sub>PG,OL</sub>  | I <sub>sink</sub> = 2mA                        |      | 0.1  | 0.3 | V     |
| Input leakage current into PG Pin | I <sub>lk(PG)</sub> | V <sub>PG</sub> = 1.8V                         |      |      | 100 | nA    |
| Output                            |                     |                                                |      |      |     |       |
| Feedback regulation voltage       | V <sub>FB</sub>     | PWM                                            | 785  | 800  | 815 | mV    |
|                                   |                     | PWM, T <sub>J</sub> = 0°C to 85°C              | 790  | 800  | 810 | mV    |
|                                   |                     | PSM                                            | 785  | 800  | 823 | mV    |
|                                   |                     | PSM, T <sub>J</sub> = 0°C to 85°C              | 788  | 800  | 812 | mV    |
| Feedback input leakage current    | I <sub>lk(FB)</sub> | V <sub>FB</sub> = 0.8 V                        |      | 1    | 100 | nA    |
| Power Switch                      |                     |                                                |      |      |     |       |
| High-side FET on-resistance       | R <sub>DS(on)</sub> | V <sub>IN</sub> ≥6V                            |      | 85   |     | mΩ    |
| Low-side FET on-resistance        |                     | V <sub>IN</sub> ≥6V                            |      | 35   |     | mΩ    |
| Low-side FET switch current limit | I <sub>LIM</sub>    | V <sub>IN</sub> = 6 V, T <sub>A</sub> = 25°C   | 3    | 3.6  | 4.2 | A     |
| PWM switching frequency           | f <sub>SW</sub>     | I <sub>OUT</sub> = 1A, V <sub>OUT</sub> = 1.8V |      | 2    |     | MHz   |

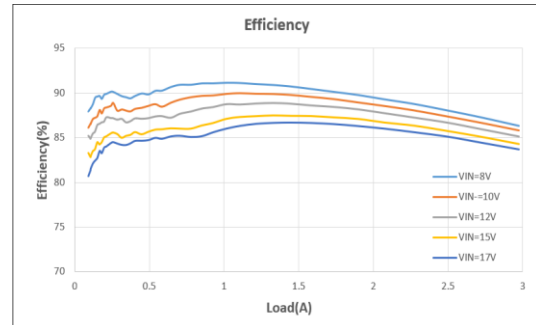
## TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

Test conditions unless otherwise noted:  $V_{IN} = 12V$ ,  $V_{OUT} = 1.0V$ ,  $C_{IN} = 2 \times 10\mu F$ ,  $C_{OUT} = 2 \times 47\mu F$  and  $T_A = +25^\circ C$ .

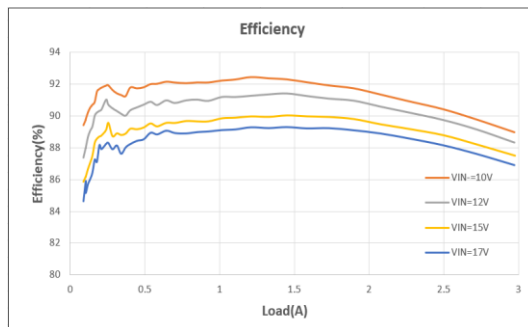
**Efficiency vs. Load Current,  $V_{OUT} = 1.0V$**



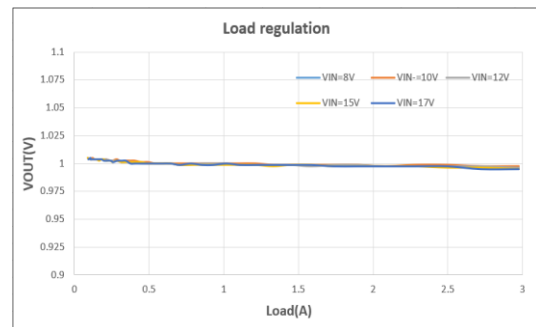
**Efficiency vs. Load Current,  $V_{OUT} = 3.25V$**



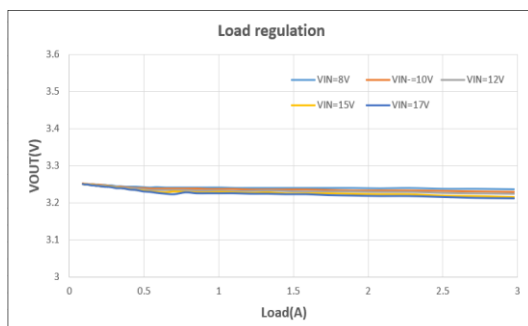
**Efficiency vs. Load Current,  $V_{OUT} = 5.05V$**



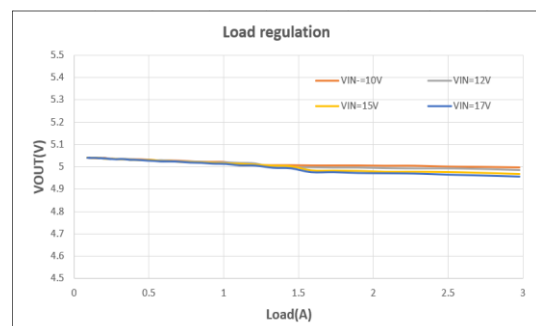
**Load Regulation,  $V_{OUT} = 1.0V$**



**Load Regulation,  $V_{OUT} = 3.25V$**



**Load Regulation,  $V_{OUT} = 5.05V$**

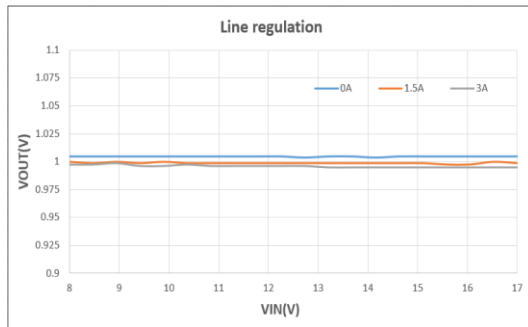


## TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

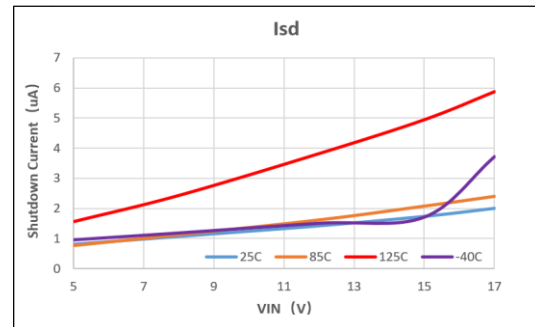
Test conditions unless otherwise noted:  $V_{IN} = 12V$ ,  $V_{OUT} = 1.0V$ ,  $C_{IN} = 2 \times 10\mu F$ ,  $C_{OUT} = 2 \times 47\mu F$  and  $T_A = +25^\circ C$ .

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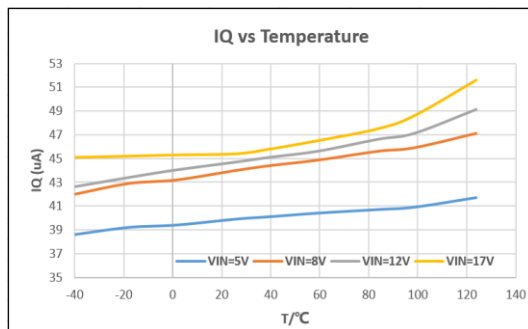
Line Regulation,  $V_{OUT} = 1.0V$



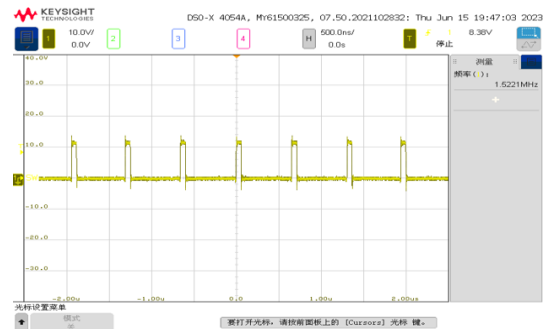
Shutdown Current



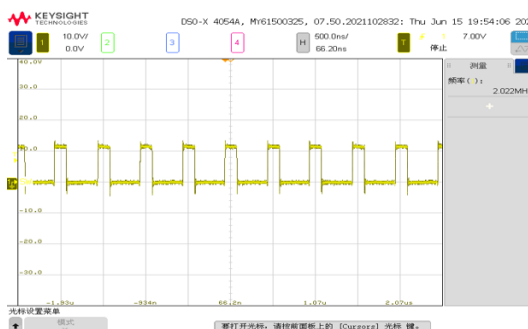
Quiescent Current



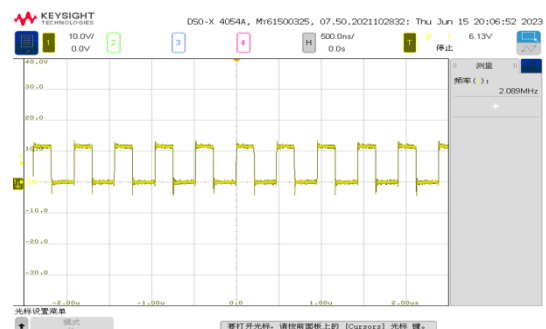
Switching Frequency,  $V_{OUT} = 1.0V$ , Load=3A



Switching Frequency,  $V_{OUT} = 3.3V$ , Load=3A



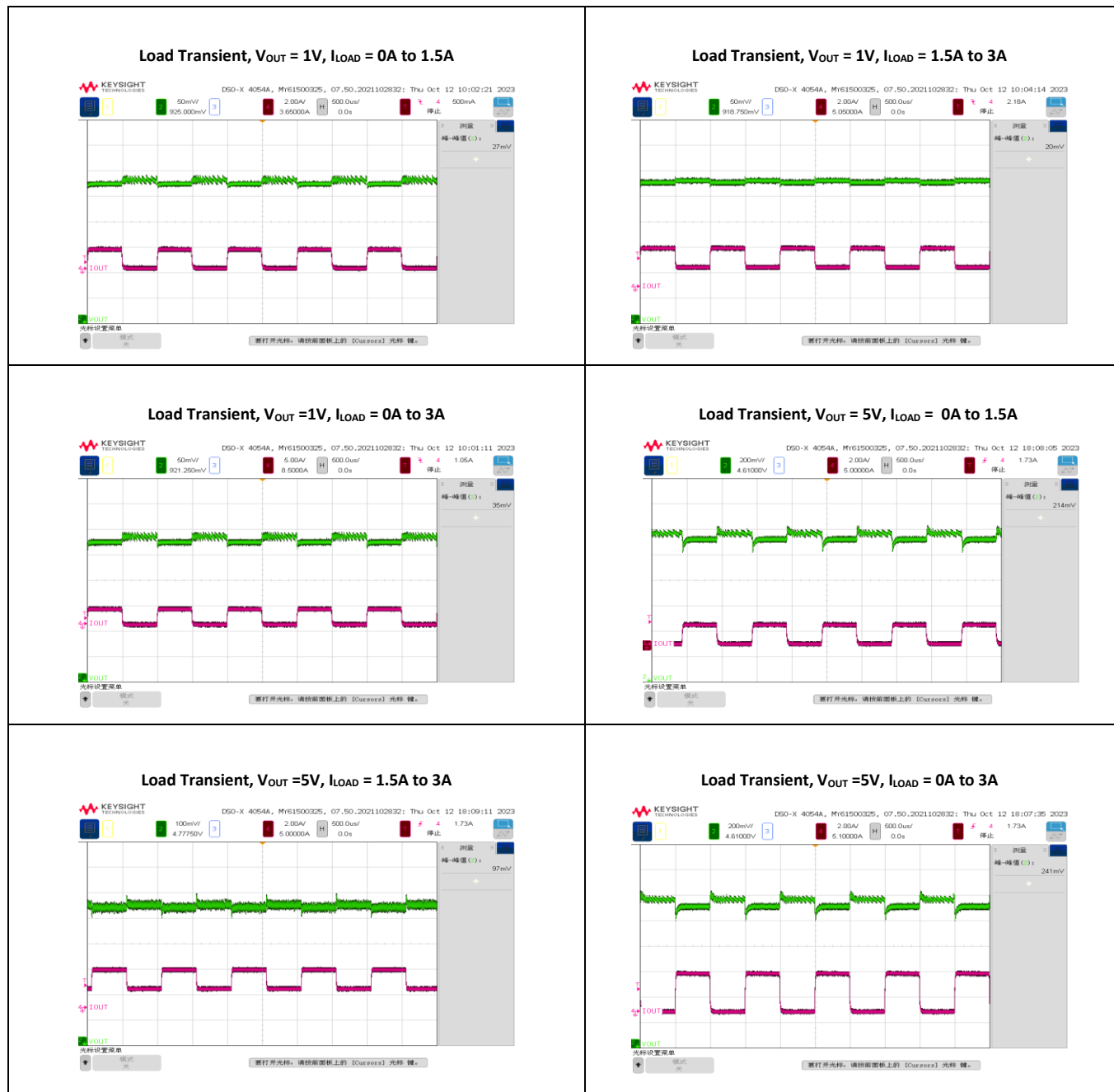
Switching Frequency,  $V_{OUT} = 5V$ , Load=3A



## TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

Test conditions unless otherwise noted:  $V_{IN} = 12V$ ,  $V_{OUT} = 1.0V$ ,  $C_{IN} = 2 \times 10\mu F$ ,  $C_{OUT} = 2 \times 47\mu F$  and  $T_A = +25^\circ C$ .

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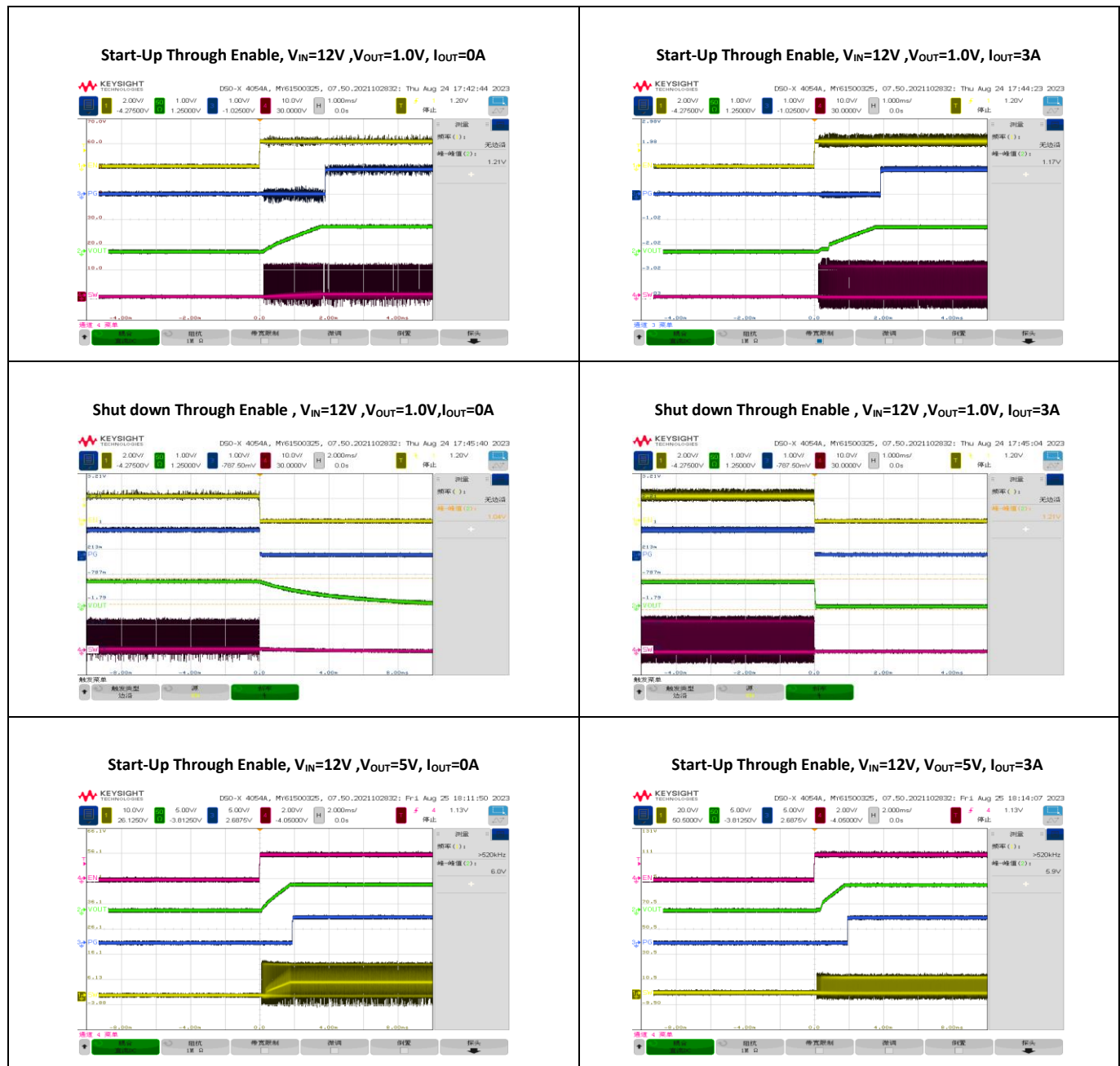


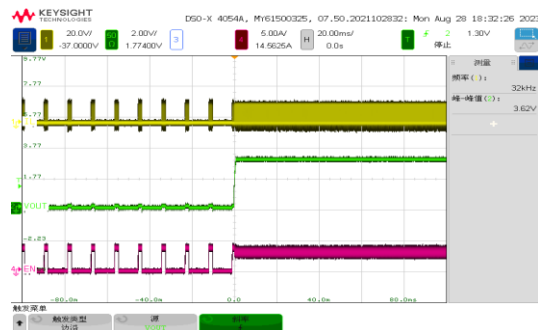
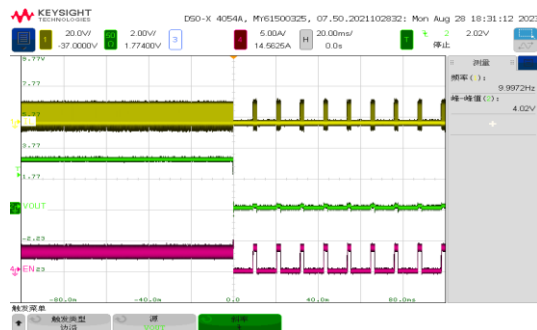
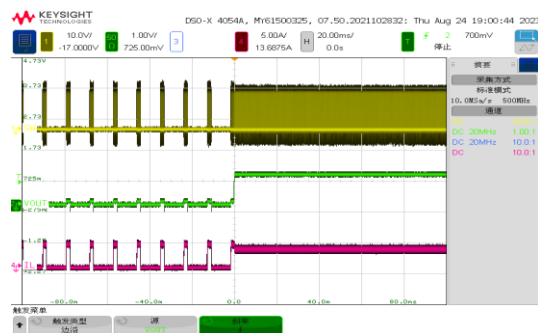
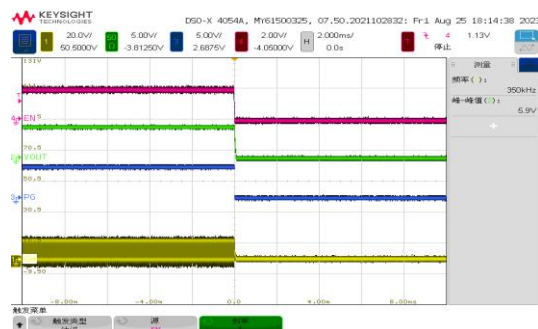
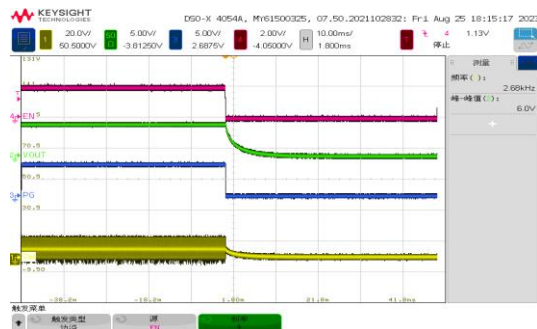


## TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

Test conditions unless otherwise noted:  $V_{IN} = 12V$ ,  $V_{OUT} = 1.0V$ ,  $C_{IN} = 2 \times 10\mu F$ ,  $C_{OUT} = 2 \times 47\mu F$  and  $T_A = +25^\circ C$ .

(continued)



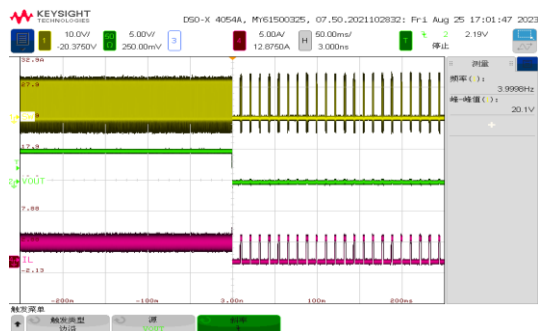


## TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

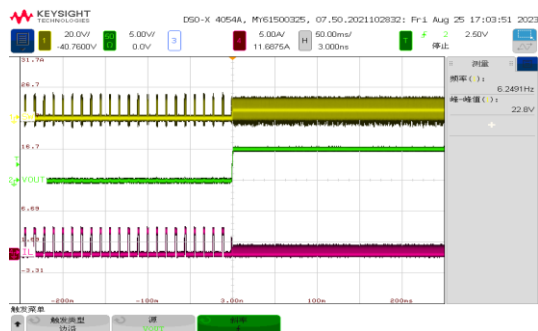
Test conditions unless otherwise noted:  $V_{IN} = 12V$ ,  $V_{OUT} = 1.0V$ ,  $C_{IN} = 2 \times 10\mu F$ ,  $C_{OUT} = 2 \times 47\mu F$  and  $T_A = +25^\circ C$ .

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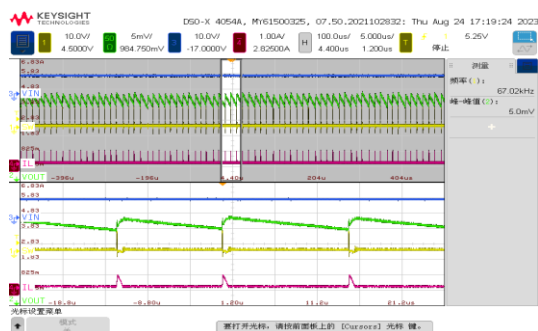
Short Circuit Protection,  $V_{IN}=12V$ ,  $V_{OUT}=5V$ , 3A to Short



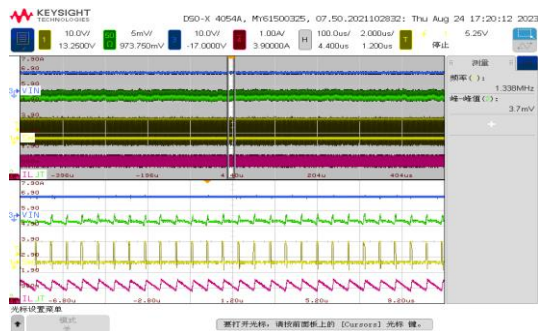
Short Circuit Recovery,  $V_{IN}=12V$ ,  $V_{OUT}=5V$ , Short to 3A



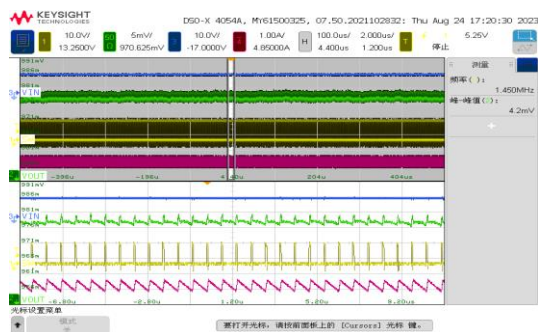
Steady State Test,  $V_{IN}=12V$ ,  $V_{OUT}=1.0V$ , Load=0A



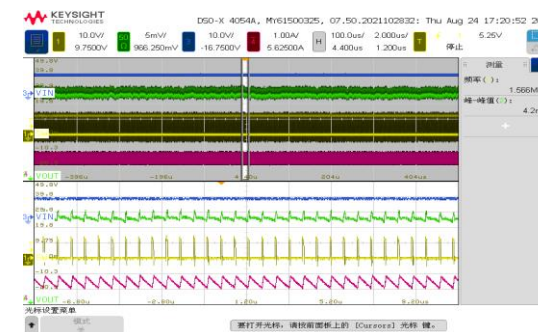
Steady State Test,  $V_{IN}=12V$ ,  $V_{OUT}=1.0V$ , Load=1A



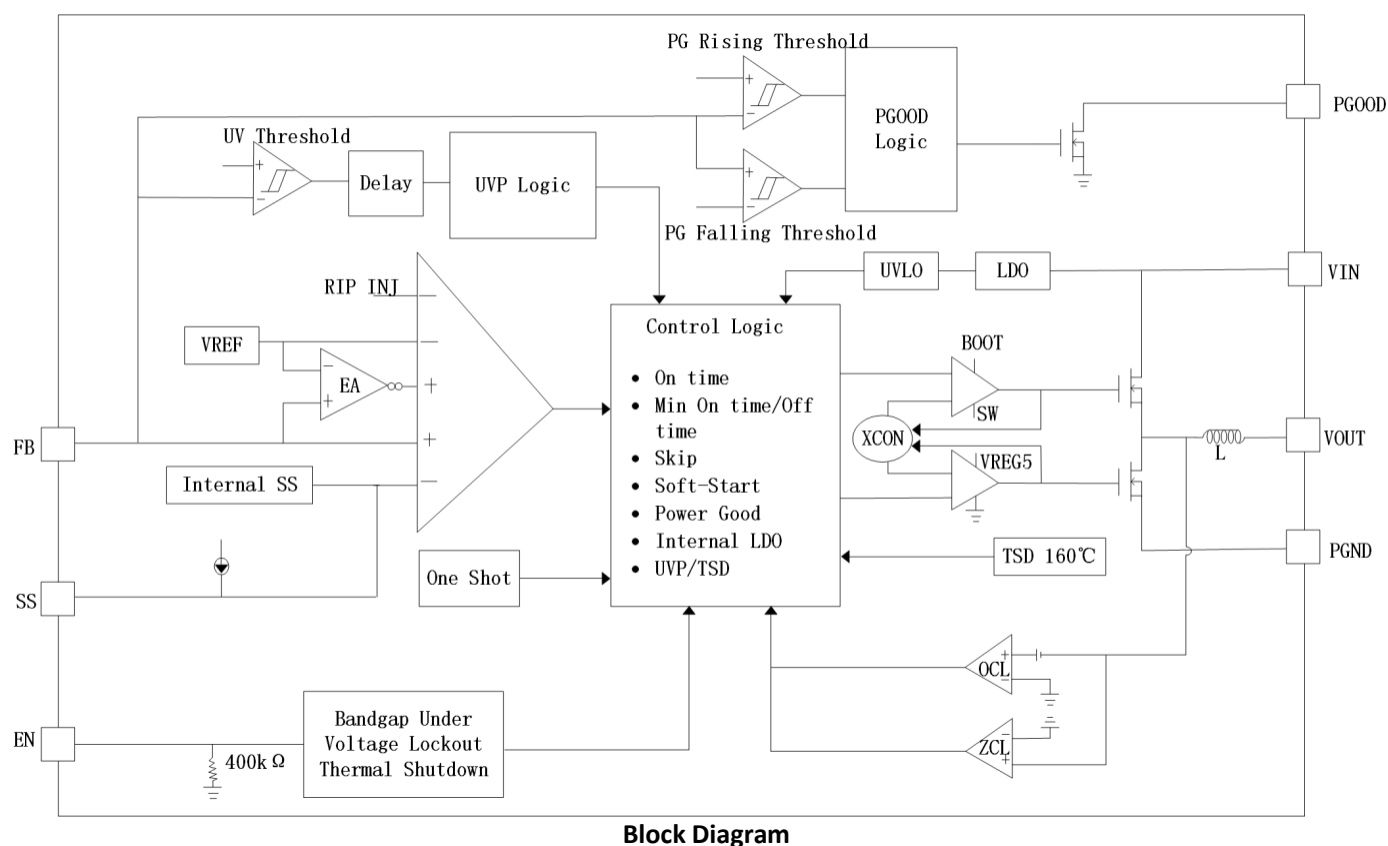
Steady State Test,  $V_{IN}=12V$ ,  $V_{OUT}=1.0V$ , Load=2A



Steady State Test,  $V_{IN}=12V$ ,  $V_{OUT}=1.0V$ , Load=3A



## FUNCTIONAL DESCRIPTION



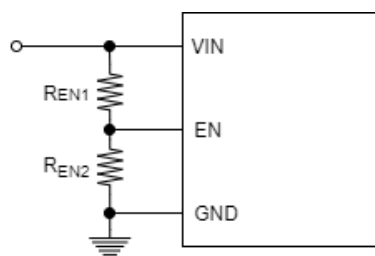
### Overview

The XPM82130 is a synchronous step-down DC-DC voltage regulator available with switching frequency of 2MHz. Operating from an input voltage between 4.5V and 17V, the regulator can deliver up to 3A of load current.

### Enable

Setting the EN pin to logic High enables the device. Alternatively, the device is disabled when the EN voltage is set to logic Low or floating. In this state the IC draws about 1.5μA of current.

The EN pin can also be applied to adjust XPM82130 Under-Voltage Lockout (UVLO) threshold with two external resistors divider from VIN to ground, please refer to the following graph for application structure.



### Soft-Start

When the device is enabled, internal soft-start circuitry causes VOUT to ramp up over a period of 1ms to limit inrush current. This feature protects a high impedance source from being pulled to a lower voltage as the device turns on. The XPM82130

is able to start into a pre-biased output capacitor. During the pre-biased start-up, both the power MOSFETs are not allowed to turn on until the internal voltage clamp sets an output voltage above the pre-bias voltage. When the device is in shutdown, under voltage lockout, or thermal shutdown, the capacitor connected to the SS pin is discharged by an internal resistor. Returning from those states causes a new start-up sequence.

A capacitance connected between the SS pin and the GND allows programming the start-up slope of the output voltage. A constant current of 2.5μA charges the external capacitor. The capacitance required for a given soft start-up time for the output voltage is given by:  $C_{ss} = T_{ss} \times I_{ss} / 1.25$ .

## Under-voltage Lockout (UVLO)

The under-voltage lockout feature prevents the device from turning on if  $V_{IN}$  is below the UVLO level of 4.2V. If the device is enabled under UVLO conditions, the circuitry will not turn on until the input voltage is increased. Once active, the UVLO circuit has 400mV of hysteresis and the device will turn off if  $V_{IN}$  drops below 3.8V.

## Thermal Shutdown

The device thermal shutdown protection is enabled if the chip temperature exceeds 160°C. Once the temperature drops below 140°C, the device will be re-enabled, and a new soft-start cycle will begin.

## Over current Protection

The device has over current protection to prevent damage to the device and inductor during over current conditions.

Valley current protection occurs at 3.6A. After  $V_{OUT}$  drops to about 60%, the output will be disabled. After being disabled for 10ms, the device will be re-enabled, and a new soft-start cycle will begin.

## Power Good Indicator

The PG pin is an open-drain output and pulls the PG pin low when the FB voltage is less than 92% of the nominal internal reference voltage and resumes when FB voltages is greater than 96% of the nominal internal reference voltage.

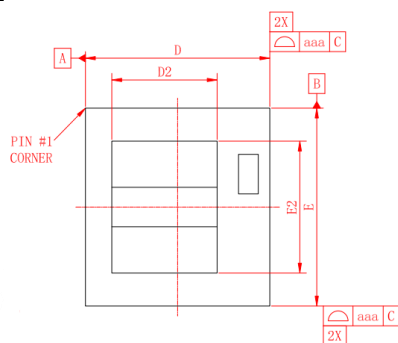
**Power Good Pin Logic**

| DEVICE STATE         |                            | PG LOGIC STATUS |     |
|----------------------|----------------------------|-----------------|-----|
|                      |                            | HIGH IMPEDANCE  | LOW |
| Enable (EN=High)     | $V_{FB} \geq V_{TH\_PG}$   | √               |     |
|                      | $V_{FB} \leq V_{TH\_PG}$   |                 | √   |
| Shutdown (EN=Low)    |                            |                 | √   |
| UVLO                 | $0.7V < V_{IN} < V_{UVLO}$ |                 | √   |
| Thermal Shutdown     | $T_J > T_{SD}$             |                 | √   |
| Power Supply Removal | $V_{IN} < 0.7V$            | √               |     |

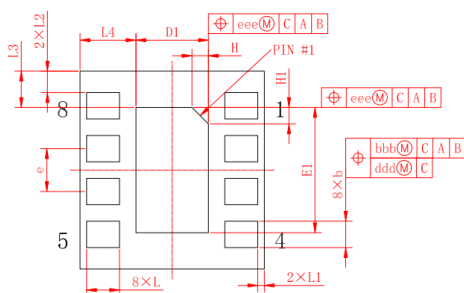
## PHYSICAL DIMENSIONS

Table: Chip Dimensions

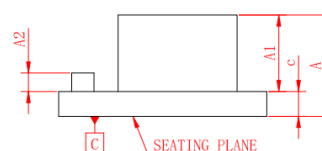
| Symbol | Dimensions in mm |       |       |
|--------|------------------|-------|-------|
|        | Min              | Nom   | Max   |
| A      | ---              | ---   | 1.410 |
| A1     | ---              | ---   | 1.040 |
| A2     | ---              | ---   | 0.260 |
| c      | 0.300            | 0.335 | 0.370 |
| D      | 2.750            | 2.800 | 2.850 |
| E      | 2.950            | 3.000 | 3.050 |
| D1     | 1.000            | 1.100 | 1.200 |
| E1     | 1.800            | 1.900 | 2.000 |
| D2     | 1.400            | 1.600 | 1.800 |
| E2     | 1.800            | 2.000 | 2.200 |
| H      | ---              | 0.250 | ---   |
| H1     | ---              | 0.250 | ---   |
| L      | 0.450            | 0.500 | 0.550 |
| L1     | 0.025            | 0.100 | 0.175 |
| L2     | 0.250            | 0.325 | 0.400 |
| L3     | 0.475            | 0.550 | 0.625 |
| L4     | 0.775            | 0.850 | 0.925 |
| e      | ---              | 0.650 | ---   |
| b      | 0.350            | 0.400 | 0.450 |
| aaa    | 0.100            |       |       |
| bbb    | 0.150            |       |       |
| ddd    | 0.080            |       |       |
| eee    | 0.150            |       |       |



Top View



Bottom View



Side View